U.S. Department of Commerce, Patent and Trademark Office	Attorney Docket No.: 023-0001
	Application No.: 09/990,901
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s): Roy Scheuerlein
(Use several sheets if necessary)	Filing Date: Nov. 16, 2001
	Group Art Unit: 2818
	Date Submitted: January 3, 2002

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
HW	AA	4,646,266	Feb. 24, 1987	Ovshinsky et al.	365	105	
	AB	5,109,360	Apr. 28, 1992	Inazumi et al.	365	200	
	AC	5,172,341	Dec. 15, 1992	Amin	365	222	
	AD	5,315,558	May 24, 1994	Hag	365	230.01	
	AE	5,367,653	Nov. 22, 1994	Coyle et al.	395	400	
	AF	5,671,229	Sep. 23, 1997	Harari et al.	371	10.2	
	AG	5,691,945	Nov. 25, 1997	Liou et al.	365	200	
	AH	5,751,012	May 12, 1998	Wolstenholme et al.	257	5	
	AI	5,764,576	Jun. 9, 1998	Hidaka et al.	365	200	
	AJ	5,805,520	Sep. 8, 1998	Anglada	365	230.02	
V	AK	5,835,396	Nov. 10, 1998	Zhang	365	51	

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

HW	AR	U.S. App. No. 09/748,649, filed Dec. 22, 2000, "Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operations," inventors Roy E. Scheuerlein and Matthew P. Crawley, 38 pp.
	AS	U.S. App. No. 09/897,705, filed June 29, 2001, "Three-Dimensional Memory Array Incorporating Serial Chain Diode Stack," inventors Bendik Kleveland et al., 72 pp.
V	AT	U.S. App. No. 09/747,574, filed Dec. 22, 2000, entitled "Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein," and naming inventors Thomas H. Lee, James M. Cleeves and Mark G. Johnson, 18 pages.

Examiner	Date Considered
Hoa T. Nguyen	3/3/05

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HV	AA	5,896,404	Apr. 20, 1999	Kellogg et al.	371	40.11	
	AB	5,999,446	Dec. 7, 1999	Harari et al.	365	185.03	
	AC	6,020,758	Feb. 1, 2000	Patel et al.	326	40	
	AD	6,034,882	Mar. 7, 2000	Johnson et al.	365	103	
	AE	6,052,798	Apr. 18, 2000	Jeddeloh	714	8	
	AF	6,055,180	Apr. 25, 2000	Gudesen et al.	365	175	
	AG	6,069,638	May 30, 2000	Porterfield	345	516	
	AH	6,070,262	May 30, 2000	Kellogg et al.	714	763	
	AI	6,081,463	Jun. 27, 2000	Shaffer et al.	365	200	
	AJ	6,149,316	Nov. 21, 2000	Harari et al.	395	182.06	
↓	AK	6,163,490	Dec. 19, 2000	Shaffer et al.	365	200	

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	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

HV	AR	U.S. Pat. App. No. 09/560,626, filed April 28, 2000, entitled "Three-Dimensional Memory Array and Method of Fabrication," naming inventor N. Johan Knall, 48 pp.
	AS	U.S. App. No. 09/638,428, filed Aug. 14, 2000, "Low Cost Three-Dimensional Memory Array," inventors Mark G. Johnson et al., 25 pp.
↓	AT	U.S. App. No. 09/814,727, filed March 21, 2001, "Three Dimensional Memory Array and Method of Fabrication," inventors Johan Knall and Mark G. Johnson, 49 pp.

Examiner Hien Nguyen	Date Considered 3/3/05

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HW	AA	6,166,559	Dec. 26, 2000	McClintock et al.	326	10	
	AB	6,192,487 B1	Feb. 20, 2001	Douceur	714	8	
	AC	6,236,602 B1	May 22, 2001	Patti	365	201	
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

HW	AR	Toshio Wada et al, "A 15-ns 1024-Bit Fully Static MOS RAM," IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 5, Oct. 1978, pp. 635-639.
	AS	Kim C. Hardee and Rahul Sud, "A Fault-Tolerant 30 ns/375 mW 16K x 1 NMOS Static RAM,"IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 5, Oct. 1981, pp. 435-443.
	AT	Misao Higuchi et al., "An 85ns 16mB MOS EPROM with Alterable Word Organization," ISSCC 90, 1990 IEEE International Solid-State Circuits Conference, Feb. 1990, pp. 56-57.
	AU	"TH58512FT Toshiba MOS Digital Integrated Circuit Silicon Gate CMOS" datasheet, 1999, 34 pp.

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